ABSTRACT

An apparatus for digitally processing signals within wireless communications base-stations which includes a channel pooling signal processor and a digital signal processor. The channel pooling signal processor includes a plurality of computation units typically realized in a heterogeneous multiprocessing architecture, a test interface for testing the function of the plurality of the computation units, a general-purpose microprocessor for managing the dataflow into and out of the channel pooling signal processor as well as effecting the control and configuration of the computation units, and an interconnect mechanism for connecting the plurality of computation units to the input, output, test interface, and the general-purpose microprocessor.